Design and Analysis of LC-VCO for Ultra Wide-Band Operation

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Abstract- A modified inductance-capacitance voltage controlled oscillator (LC-VCO) topology is presented in this paper. NMOS only varactor has been used instead of variable capacitance. The frequency of oscillation of the VCO is 7.68GHz with a power dissipation of 5.68mW. The designed oscillator is characterized by a tuning range of 26.73%. Compared to the reference circuit, there is an improvement in frequency of oscillation of the LC-VCO. The design is verified using SPICE simulations.

Key Words- Inductance Capacitance-Voltage Controlled Oscillator, Ultra-wideband frequency, VCO.

1. Introduction

The growing demand for higher data transfer rates and lower power consumption has a major impact on the design of radio frequency (RF) communication systems. In both wireless and wired applications, this has been achieved using more spectrally efficient modulations and wider channel bandwidth in combination with engineering techniques to lower power and fabrication costs. Furthermore, as communication standards evolve and new applications are created, systems have to cope with a more crowded spectrum. This has resulted in a trend promoting more wideband and spectrally adaptive devices. Fig. 1 shows the distribution of ultra wide band (UWB) frequency bands [1]. There are many architectures of voltage controlled oscillator (VCO) but for the reason that design of LC-voltage controlled oscillators has posed several challenges to circuit designers, there is a growing interest in investigating these circuits [2-4].

![Fig. 1. Allocation of UWB frequency bands](image)

Several researchers have proposed high frequency VCOs. Long proposed a 2.4GHz low-power low-phase-noise CMOS LC-VCO [5]. A 1.4GHz CMOS LC low phase noise VCO using tapped bond wire inductances is presented by Ahrens and Lee [6]. A 1V, 5GHz low phase noise LC-VCO using voltage-dividing and bias-level shifting technique is proposed by Song [7]. An optimized analytical design of a 2.5GHz CMOS VCO is given by Dehghani and Atarodi [8]. Graphically optimized design of a 4GHz CMOS LC-VCO is reported by Issa et al [9].

Even though significant amount of research work related to VCO design has been carried out, VCO is still a challenging component amongst RF complementary metal oxide semiconductor (CMOS) very large scale integration (VLSI) designers [10-12]. The same has been attempted in this work.

2. Voltage Controlled Oscillator topologies

VCO is an electronic circuit designed to be controlled in oscillation frequency by a voltage input. The oscillator requires a tank circuit. A parallel resonance tank comprises of inductance (L) and capacitance (C). The principle operation of the VCO is by means of the controlled operation of the LC tank circuit. A general LC tank circuit [2] is shown as in Fig. 2. In Fig. 2, RL and RC are the parasitic resistances associated with L and C respectively. In order to compensate the losses due to RL and RC, active components like MOS transistors are used to realize the negative resistance (-R) shown in Fig. 2 [2].

![Fig. 2. Basic LC tank circuit](image)
active negative-resistance circuit of cross-couple is shown in the Fig. 3.

![Fig. 3. Traditionally active negative-resistance cross-couple topology](image)

The equivalent capacitance and transconductance for the cross-coupled topology shown in Fig. 3 are given by [4]:

\[
C_{NMOS} = C_{gr,n} + C_{db,b} + 4C_{gd,n} \tag{1}
\]

\[
g_{tank} = \frac{1}{2} \left( g_{ds} + g_t + g_v + g_{sw} \right) \tag{2}
\]

where \(C_{gr,n}, C_{gd,b}\) and \(C_{gd,n}\) are the gate-source, drain-bulk and gate-drain capacitances respectively. Furthermore, \(g_{ds}, g_t, g_v\) and \(g_{sw}\) are the output conductance of the transistor, conductance of inductor, conductance of tuning varactors and conductance of switch varactors, respectively [4]. Fig. 4 shows varactor using NMOSFETs only by connecting the drain and source to each other in order to implement capacitance. In the similar way four such capacitors are being implemented by using NMOS M1, M2, M3 and M4 connected as a varactor.

![Fig. 4. Varactor using NMOS only](image)

Advantage of CMOS topology is that the tank amplitude is twice that of the NMOS-only topology for a given current. Secondly, it can be optimized to have more symmetry in the output waveform leading to noise reduction. Also the LC- VCO consumes less power for a given phase noise [13-15]. The superiority is also due to the fact that CMOS structures provide higher transconductance for a given bias current, which results in faster switching of the cross-coupled differential pair. CMOS topologies have better rise and fall time symmetry [2]. Fig. 5 shows varactor with M11 and M12 connected in cross-coupled configuration to implement negative resistance in order to further reduce resistance. Transistors M5, M6, M7, M8, M9 and M10 are used to implement negative resistance. The equivalent admittance and capacitance of the traditional negative resistance circuit is given by eqs (3) and (4) respectively [4].

\[
Y_{in} = SC_{in} - g_{m1} \tag{3}
\]

\[
C_{in} = C_{db1} + C_{gd2} + C_{gd1} (1 - \frac{1}{K1}) + C_{gd2} (1 - K2) \tag{4}
\]

Since the transistors M1 and M2 are matched, therefore the gain based on Miller’s theorem \(k1= k2= -1\), it can be seen that \(C_{NMOS} = C_{gr,n} + C_{db,b} + 4C_{gd,n}\). In order to enhance the tuning range of VCO, \(C_{in}\) input capacitance of traditional NMOS circuit should be minimized. Therefore, a negative-resistance used with varactor in the circuit reduces the parasitical capacitances [4]. Where, it is found that

\[
C_1 = C_{gd3} + C_{db3} + C_{gd1}
\]
\[ C_3 = C_{db1} + C_{gs3} + C_{ds3} + C_{gd5} + C_{db5} \]

From the analysis of circuit it is seen that admittance of the circuit can be given by [3]

\[ Y_m = S(C_1 + C_{gs1}) - \frac{(SC_{gs1} + g_m)(SC_{gs1} + g_{m3})}{S(C_{gs1} + C_3) + g_m + g_{m3}} \quad (5) \]

From equations (3) and (5) it is clear that the proposed circuit has smaller input capacitance than the traditional negative-resistance circuit. It leads to wider tuning-range than that the LC-VCO circuit can achieve. Also the transconductance of the LC-VCO circuit can be written as

\[ G_m = \frac{g_m g_{m3}}{(g_m + g_{m3})} \quad (6) \]

Since transistors M5, M6, M3, M8, M9 and M10 are connected to implement negative resistance. A traditional negative-resistance circuit is paralleled with this negative-resistance circuitry. This leads to larger total transconductance which is sufficient enough to raise the oscillations. Besides, the parasitical capacitance of this modified negative-resistance circuit is larger than the conventional negative resistance circuit. The transconductance kept large enough so that the tuning range is wider than using the traditional negative-resistance circuit. The varactor is also used by using NMOS-only circuit to further increase its tuning range [13]. The transconductance \( g_{m7,8} \) is the equivalent transconductance and \( \omega_0 \) is the frequency of oscillation of the modified design are given as [2-4]:

\[ g_{m7,8} = \frac{2}{R_p} + \frac{2}{j\omega_0 L_p} + 
\frac{j\omega_0 (C_{var} + C_{7,8} + 4C_{gd7,8}) + Y_m}{j\omega_0 (C_{var} + C_{7,8} + 4C_{gd7,8}) + Y_m} \quad (7) \]

and

\[ \omega_0 = \sqrt{\frac{2a}{L_p R_p [b - cd - e] - f}} \quad (8) \]

where,

\[ a = R_p (g_{m1} + g_{m3}) \]
\[ b = g_{m7,8} (C_{gs1} + C_3) \]
\[ c = (C_{var} + C_{7,8} + 4C_{gd7,8}) \]
\[ d = (g_m + g_{m3}) \]
\[ e = C_1 (g_m + g_{m3}) \]
\[ f = L_d (C_{gs1} + C_3) \]

It can be seen and appreciated from eqs. (2) to (7) that transconductance of the modified design is sufficiently high for the oscillator to operate in ultra wide band.

3. Results and Discussion

The modified VCO considered in this work has been simulated and its performance is analyzed. SPICE simulations are carried out for 180nm technology node for supply voltage 1.8V [15-16]. The phase noise of the LC-VCO has been analyzed. Phase noise is the frequency domain representation of rapid, short-term, random fluctuations in the phase of a waveform, caused by time domain instabilities. For this linear time varying (LTV) noise model has been used to calculated noise [2].

\[ L(\Delta f) = 10 \log \left[ \frac{2kT}{P_{sig}} \left( \frac{f_0}{2Q \Delta f} \right)^2 \right] \quad (10) \]

Fig. 6 shows LTI phase noise using eq(10). The offset frequency \( f_o \) been varied from 1Hz to 1kHz. The phase noise can be approximated at an offset of 1kHz as -175 dBc/Hz.

![Fig. 6. Phase Noise of the Proposed LC-VCO](image-url)

Figure of merit (FOM) takes all important VCO parameters like power, phase noise and oscillation frequency into account. FOM is given as [5]:

\[ FOM = 20 \log(f_0 / \Delta f) - L(\Delta f) - 10 \log P \quad (11) \]

Using eq(11) in order to decide the roll-off between various improvement constraints the FOM factor has been evaluated for frequency of oscillation of 7.68GHz with a power dissipation of 5.68mW and a phase noise of -175 dBc/Hz at 1kHz offset. FOM is found out to be 185.
The tuning range of nearly 26.73% in the frequency of oscillation with control voltage varying from 0.5V to 1.8V of LC-VCO is obtained as seen in Fig. 7.

4. Conclusions

The modified VCO presented in this work is implemented in CMOS TSMC 0.18µm process and is designed using a negative-resistance accompanied by NMOS-only varactor to increase the tuning range. In addition to the reduced supply voltage and achieving low power consumption, the proposed technique also improves the phase noise. The phase noise is -175 dBc/Hz at 1kHz offset, the tuning range is 6.06GHz~7.68GHz (26.73%) and the power consumption is 5.68 mW for 1.8V supply voltage.

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